AMENDMENT

Please amend the application as follows:

IN THE CLAIMS

Please amend claim 1, 21, and 41 as indicated below. The status and text of the claims follows:

1. (Currently amended) A programmable logic device (PLD), the programmable logic device (PLD) comprising configuration circuitry, the configuration circuitry adapted to receive serial configuration data, wherein the configuration circuitry ~~further adapted~~ is configured to program a function of the programmable logic device (PLD) without using an input buffer to store the configuration data.

2. (Original) The programmable logic device (PLD) according to claim 1, wherein the configuration circuitry receives the serial configuration data from a configuration device external to the programmable logic device (PLD).

3. (Original) The programmable logic device (PLD) according to claim 2, wherein the function of the programmable logic device (PLD) is programmed without stalling the configuration device.

4. (Original) The programmable logic device (PLD) according to claim 1, wherein the function of the programmable logic device (PLD) is programmed in an active configuration mode.

5. (Original) The programmable logic device (PLD) according to claim 1, wherein the function of the programmable logic device (PLD) is programmed in a passive configuration mode.

6. (Original) The programmable logic device (PLD) according to claim 5, wherein the configuration circuitry is further adapted to receive compressed serial configuration data.

7. (Original) The programmable logic device (PLD) according to claim 6, wherein the configuration circuitry comprises a decompression circuitry, the decompression circuitry adapted to decompress the compressed serial configuration data into decompressed configuration data.

8. (Original) The programmable logic device (PLD) according to claim 7, wherein the configuration circuitry further comprises a data format converter circuit, the data format converter circuit adapted to convert the decompressed configuration data into parallel configuration data.

9. (Original) A data-processing system, comprising:

a configuration device, the configuration device adapted to provide serial configuration data; and

a programmable logic device (PLD), comprising:

a data converter circuit, the data converter circuit adapted to convert the serial configuration data into parallel configuration data to program a function of the programmable logic device (PLD),

wherein the function of the programmable logic device (PLD) is programmed without stalling the configuration device.

10. (Original) The data-processing system according to claim 9, wherein the serial configuration data comprises serial compressed data.

11. (Original) The data-processing system according to claim 10, wherein the data converter circuit comprises a decompression circuit, the decompression circuit adapted to decompress the serial compressed data to provide decompressed data.

12. (Original) The data-processing system according to claim 11, wherein the data converter further comprises a data format converter circuit, the data format converter circuit adapted to transform the decompressed data into parallel data.

13. (Original) The data-processing system according to claim 12, wherein the parallel data is used to program the function of the programmable logic device (PLD).

14. (Original) The data-processing system according to claim 13, wherein the decompression circuitry comprises a decompression state machine.

15. (Original) The data-processing system according to claim 14, wherein the data converter further comprises a first register, the register adapted to receive the serial compressed data in response to a clock signal.

16. (Original) The data-processing system according to claim 15, wherein the data converter further comprises a plurality of registers, each of the plurality of registers adapted to receive the serial compressed data in response to a respective control signal provided by the decompression state machine.

17. (Original) The data-processing system according to claim 16, wherein the data format converter circuit comprises a multiplexer, the multiplexer coupled to the plurality of registers and to the decompression state machine.

18. (Original) The data-processing system according to claim 10, wherein the configuration device comprises a FLASH memory.

19. (Original) The data-processing system according to claim 10, wherein the function of the programmable logic device (PLD) is programmed in a passive configuration mode.

20. (Original) The data-processing system according to claim 19, wherein the configuration device provides a control signal to the programmable logic device (PLD).

21. (Currently amended) A data-processing system, comprising:

a configuration device, the configuration device adapted to provide serial configuration data; and

a programmable logic device (PLD), comprising:

a data converter circuit, the data converter circuit adapted to convert the serial configuration data into parallel configuration data to program a function of the programmable logic device (PLD),

wherein the programmable logic device (PLD) is configured to be programmed without using a buffer to store the serial configuration data before processing of the configuration data by the data converter circuit.

22. (Original) The data-processing system according to claim 21, wherein the serial configuration data comprises serial compressed data.

23. (Original) The data-processing system according to claim 22, wherein the data converter circuit comprises a decompression circuit, the decompression circuit adapted to decompress the serial compressed data to provide decompressed data.

24. (Original) The data-processing system according to claim 23, wherein the data converter further comprises a data format converter circuit, the data format converter circuit adapted to transform the decompressed data into parallel data.

25. (Original) The data-processing system according to claim 24, wherein the parallel data is used to program the function of the programmable logic device (PLD).

26. (Original) The data-processing system according to claim 25, wherein the decompression circuitry comprises a decompression state machine.

27. (Original) The data-processing system according to claim 26, wherein the data converter further comprises a first register, the register adapted to receive the serial compressed data in response to a clock signal.

28. (Original) The data-processing system according to claim 27, wherein the data converter further comprises a plurality of registers, each of the plurality of registers adapted to receive the serial compressed data in response to a respective control signal provided by the decompression state machine.

29. (Original) The data-processing system according to claim 28, wherein the data format converter circuit comprises a multiplexer, the multiplexer coupled to the plurality of registers and to the decompression state machine.

30. (Original) The data-processing system according to claim 22, wherein the configuration device comprises a FLASH memory.

31. (Original) The data-processing system according to claim 22, wherein the function of the programmable logic device (PLD) is programmed in an active configuration mode.

32. (Original) The data-processing system according to claim 22, wherein the function of the programmable logic device (PLD) is programmed in a passive configuration mode.

33. (Original) A programmable logic device (PLD), comprising:

means for receiving serial, compressed configuration data;

means for decompressing the serial, compressed configuration data to provide decompressed data; and

means for converting the decompressed data into parallel configuration data.

34. (Original) The programmable logic device (PLD) according to claim 33, further comprising means for programming a function of the programmable logic device (PLD) by using the parallel configuration data.

35. (Original) The programmable logic device (PLD) according to claim 34, wherein programming the function of the programmable logic device (PLD) comprises programming a programmable logic circuit.

36. (Original) The programmable logic device (PLD) according to claim 34, wherein programming the function of the programmable logic device (PLD) comprises programming a programmable interconnect.

37. (Original) The programmable logic device (PLD) according to claim 35, wherein the function of the programmable logic device (PLD) is programmed in an active configuration mode.

38. (Original) The programmable logic device (PLD) according to claim 35, wherein the function of the programmable logic device (PLD) is programmed in a passive configuration mode.

39. (Original) The programmable logic device (PLD) according to claim 36, wherein the function of the programmable logic device (PLD) is programmed in a passive configuration mode.

40. (Previously presented) The programmable logic device (PLD) according to claim 36, wherein the function of the programmable logic device (PLD) is programmed in a active configuration mode.

41. (Currently amended) A method of configuring a programmable logic device (PLD), the method comprising:

receiving serial configuration data by using a circuit that is configured to program a function of the programmable logic device (PLD) without using an input buffer to store the

configuration data, wherein the serial configuration data ~~being~~ is adapted to configure a function of the programmable logic device (PLD); and

configuring the function of the programmable logic device (PLD) by using the serial configuration data~~,~~

~~wherein the programmable logic device (PLD) is configured without buffering the serial configuration data~~.

42. (Original) The method according to claim 41, wherein receiving serial configuration data further comprises receiving serial configuration data from a configuration device external to the programmable logic device (PLD).

43. (Original) The method according to claim 42, wherein configuring the function of the programmable logic device (PLD) further comprises configuring the function of the programmable logic device (PLD) without stalling the configuration device.

44. (Original) The method according to claim 41, wherein configuring the function of the programmable logic device (PLD) further comprises performing the configuration in an active mode.

45. (Original) The method according to claim 41, wherein configuring the function of the programmable logic device (PLD) further comprises performing the configuration in a passive mode.

46. (Original) The method according to claim 45, wherein receiving serial configuration data further comprises receiving compressed serial configuration data.

47. (Original) The method according to claim 46, wherein configuring the function of the programmable logic device (PLD) further comprises decompressing the compressed serial configuration data to provide decompressed configuration data.

48. (Original) The method according to claim 47, wherein configuring the function of the programmable logic device (PLD) further comprises converting the decompressed configuration data into parallel configuration data.

49. (Original) The method according to claim 48, wherein configuring the function of the programmable logic device (PLD) further comprises using the parallel configuration data to configure programmable logic.

50. (Original) The method according to claim 48, wherein configuring the function of the programmable logic device (PLD) further comprises using the parallel configuration data to configure programmable interconnect.